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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,731	03/09/2004	Andy C. Wei	2000.093282	1745

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J. Mike Amerson
WILLIAMS, MORGAN & AMERSON, P.C.
Suite 1100
10333 Richmond
Houston, TX 77042

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,731	WEI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/9/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) was submitted on 03/09/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The abstract of the disclosure is objected to because it contains too many words. See MPEP § 608.01(f). The abstract should be a brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. Correction is required. See MPEP § 608.01(b).

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction and clarification of the following is required: The limitation, in claim 11, requiring a "dopant concentration of at least approximately 10^{19} ions/cm^3" does not appear to be disclosed anywhere in the specification, only 10^{18} is disclosed. Therefore, for the purpose of examination, on the merits, the examiner has regarded 10^{19} as a typographical error.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 10, 11, 15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al. US Patent 5,926,703.

6. Yamaguchi discloses the semiconductor device as claimed. See **figures 1-15** and corresponding text, where Yamaguchi teaches a device comprising: a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate **1**, a buried oxide layer **2** and an active layer **3**, the transistor being comprised of a gate electrode **8**, the bulk substrate being doped with a dopant material at a first concentration level (**col. 13, lines 5-10**), and a first doped region **11** formed in the bulk substrate, the first doped region being comprised of a dopant material that is the same type as the substrate dopant material, the first region having a greater concentration level of dopant material than the first concentration level (**col. 12, lines 63-65**), the first doped region being substantially aligned with the gate electrode.

7. Pertaining to claim 3, Yamaguchi teaches the device, wherein the transistor is comprised of a least on an NMOS and PMOS device. (ex. **figure 11**)

8. Pertaining to claim 10, Yamaguchi teaches the device, wherein the bulk substrate is doped with a P-type dopant material at a concentration of approximately 10^{15} ions/cm^3 and the first doped region is doped with a P-type dopant material at a dopant concentration of at least approximately 10^{16} ions/cm^3. (**col. 12, lines 63-65, col. 13, lines 5-7**)

9. Pertaining to claim 11, Yamaguchi teaches the device, wherein the bulk substrate is doped with an N-type dopant material at a concentration of approximately 10^{15} ions/cm^3 and the first doped region is doped with an N-type dopant material at a dopant concentration of at least approximately 10^{19} ions/cm^3, taking into consideration, that "10^{19}" is not disclosed in the specification and that this is taken to be a typographical error. (**col. 14, lines 51-55**)

10. Pertaining to claim 15, Yamaguchi teaches the device, wherein the first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between the buried oxide layer and the bulk substrate.(ex. **figure 1,** see center portion of **11**)

11. Pertaining to claim 17, Yamaguchi teaches the device, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections. (ex. **figure 11**)

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 2, 4-14, 16, and 18-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. US Patent 6,221,724 in view of Yamaguchi et al. US Patent 5,926,703.

14. Yu shows the semiconductor device substantially as claimed . Pertaining to claims 1, 2, 7, 18, 23, and 31, see **figures 1-6** and corresponding text, where Yu teaches a device, comprising: a transistor comprised of a bulk substrate **12**, the transistor being comprised of a gate electrode **22**, the bulk substrate being doped with a dopant material at a first concentration level (**col. 5, lines 1-5**), and a first doped region **36** formed in the bulk substrate, the first doped region being comprised of a dopant material that is the same type as the substrate dopant material, the first region having a greater concentration level of dopant material than the first concentration

level (**col. 7, lines 30-34**), the first doped region being substantially aligned with the gate electrode.

15. Yu teaches the device, further comprising second and third doped regions **40, 42** formed in the substrate **12**, the second and third doped regions being comprised of a dopant material that is the same type as the bulk substrate dopant material (**col. 5 lines 64-67, col. 6 lines 1-7**), the second and third doped regions having a greater concentration level of dopant material than the first concentration level, the first doped region being vertically spaced apart form the second and third doped regions by a distance that corresponds approximately to the thickness of the gate electrode (**col. 5, lines 5-62**). Pertaining to claims 14, 27, and 39, Yu teaches the device, wherein each of the second and third doped regions has an inner edge that is approximately aligned with respect to the gate electrode (ex. **Figure 1**). Finally, pertaining to claims 30 and 42, Yu teaches the device, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections. (ex. **Figure 1**)

16. However, Yu fails to show, pertaining to claims 1, 8, 9, 16, 18, 28, 29, 31, 36, 37, 40, and 41, the device being a transistor formed above a silicon-on-insulator substrate comprised of a buried oxide layer and an active layer, and wherein the first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between the buried oxide layer and the bulk substrate. In addition, Yu fail to teach wherein the bulk substrate is doped with a P-type and/or N-type dopant material at a concentration of approximately 10^{15} ions/cm^3 and the first, second and third doped regions are doped with a P-type and/or N-type dopant material at a dopant concentration of at least approximately 10^{16} ions/cm^3.

17. Yu also fails to show, pertaining to claims 4-6, 12, 13, 20-22, 24-26, 33-35 and 38, the device, wherein the buried oxide layer has a thickness ranging form approximately 5-50 nm, the active layer having a thickness of approximately 5-30 nm, the gate electrode having a thickness of approximately 100-150 nm, (first, second, third) doped regions having a thickness of approximately 10-50 nm, and finally wherein the bulk substrate is doped with an N-type material at a dopant concentration of at least approximately 10^{19} ions/cm^3.

18. Yamaguchi teaches in **figures 1-15** and corresponding text, pertaining to claims 8, 9, 16, 18, 28, 29, 31, 36, 37, 40, and 41, a semiconductor device using a silicon on insulator substrate (SOI) having a buried oxide layer where a high concentration region is extended under the channel formation region between the buried oxide layer and the bulk substrate thickness ranging form approximately 5-50 nm and the specific ranges of thickness and doped impurity concentrations.

19. It would have been obvious to one of ordinary skill in the art to incorporate the SOI features including the buried oxide and active layer according to the teachings of Yamaguchi, into the Yu semiconductor device, with the motivation that, as stated in Yu, **col. 1, lines 15-18**, the use of an SOI substrate produces faster switching speed of the transistor due to shorter transit time or carrier movement between source/drain regions. Additionally, as stated in **col. 13, lines 10-30 and col. 16, lines 6-13**, Yamaguchi teaches that since the high concentration region **11** is formed under the silicon substrate **1**, the short channel effect, caused by the rise of potential in the interface of the channel formation region **11** on the buried oxide region film **2,** which is caused by the depletion layer **16,** has now been prevented and the leakage current is not increased. Finally, the channel formation region **4** and the high concentration region **11,** having

the same conductive type, also prevents the short channel effect resulting from a rise in potential in the buried oxide layer.

20. It would have been obvious to one of ordinary skill in the art to incorporate the claimed ranges with regards to thickness and doped impurity concentration, pertaining to claims 4-6, 12, 13, 20-22, 24-26, 33-35 and 38, as stated in **col. 14, lines 22-23, col. 16, lines 33-42**, in the method of Yu in view of Yamaguchi, with the motivation that these ranges are within the same order of the ranges taught in both Yu and Yamaguchi.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
July 14, 2004

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812